**AI’s Intrude into IC Design: Will It Drive out Design Engineers?**

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With the advancement of AI in recent years, how to apply AI to chip design has become a hot topic in the semiconductor industry. As relevant discussions unfold, the entry point of AI's empowerment of the chip industry is increasingly focused on the field of EDA, that is, how to use the powerful capabilities of AI to help realize chip design, verification and testing more efficiently. . Since AI began to take off in 2016, there have been two landmark events, namely AlphaGO , which used a reinforcement learning model and defeated Lee Sedol, and the recent emergence of ChatGPT, which is based on large language model technology. Interestingly, these two technologies are also the key technologies for AI to empower EDA.

**AI and EDA Technology**

In the field of EDA, the area where AI has received the most attention is how to optimize design. Design optimization here refers to how to efficiently search for the optimal solution in a design space with a huge search space. Specific tasks here can include optimal placement and routing, as well as input combinations for verification and testing.

Regarding AI solutions to these problems, the current industry can be roughly divided into two categories. The first category is giants that are large enough and have strong AI research and development capabilities and chip design process customization capabilities. Such giant companies can have the ability to independently develop related AI technologies and apply them in self- developed chip design processes to improve the efficiency of the design process and chip quality. Among such companies, the most representative is Google. Google has the world's leading AI team, and also has a self- developed chip TPU. The most important thing is that Google's team is also very keen to apply AI to various new application scenarios, so Google uses AI to improve the chip. The design is also reasonable. According to Google's paper " A graph placement methodology for fast chip design" published in the "Nature" , we know that it has applied AI to greatly improve the layout and routing capabilities of self-developed chips . It uses reinforcement learning model placement and routing. The performance achieved by the algorithm has surpassed the results of manual placement and routing. The most important thing is that this technology has been used in multiple generations of Google TPU. In other words, Google uses AI to design self- developed AI chips (TPUs), which are used to further train more powerful AI to design next-generation AI chips - such a forward cycle currently seems at least It’s already starting to take shape on Google’s side .

In addition to Google , Nvidia has also accumulated a lot of experience in AI placement and routing technology. The research results published by its research team last month showed that its self- developed AI algorithm DREAMPlace / AutoDMP can complete the 256 core RISC-V processor layout tasks in 2.5 hours and exceeds the performance of other related algorithms. Of course, the AI model here runs on Nvidia's powerful multi-card GPU server. Although Nvidia has not clearly stated the commercialization status of this self-developed AI layout algorithm, we believe that it is very promising to improve when it matures enough to improve design efficiency and quality for the next generation of Nvidia GPUs.

In addition to the above, another industry players making important moves are the traditional EDA vedors. Both Cadence and Synopsys have announced their heavy investment in AI research and development for several years, and recently Cadence and Synopsys have released related products. At the SNUG 2023 held not long ago, Synopsys released a new generation of EDA tools driven by AI called Synopsys.ai, which includes DSO.ai for optimizing design, efficiently generating verification vectors and improving debugging efficiency. VSO.ai, and TSO.ai for generating test vectors. According to official data from Synopsys, DSO.ai is mainly used to improve the optimization of the design space to achieve PPA improvement. Currently, there are 160 chips using DSO.ai tape-out . DSO.ai can achieve up to 15% power reduction, and significantly reduce design time (up to three times). Using VSO.ai and TSO.ai, users can also greatly reduce the time required for verification and testing and improve efficiency. Cadence also released Allegro X in early April, whose AI features can automatically and efficiently generate the layout of PCB designs and the routing of key signals, thereby reducing design time.

If design /verification optimization is the area of greatest concern for traditional EDA tools, then another important aspect that has not received enough attention in traditional EDA tools is design input, especially RTL code writing assistance related to digital logic design. This field has always been considered to be possible using any text editor, so it has always been out of the sight of EDA companies; but recently, with the popularity of large language models and the use of large language models to provide assistance in writing computer code such as Python Copilot is being used more and more. In fact, using similar copilot technology in RTL code writing is becoming a potentially popular direction. Copilot technology automatically prompts and completes possible codes based on the context in which users write code, thereby reducing the amount of code that users need to enter and reducing the possibility of bugs during user code writing, thereby greatly increasing the efficiency of user code writing. In the future, as the improvement in capabilities can even increasingly automate RTL code writing, so that users only need to give a short prompt, and AI can give a code draft for the user to use.



In summary, the EDA industry has officially entered the AI era, and we are expected to see the emergence of more AI-empowered EDA in the future.

**The Core Technology Behind AI EDA**

As mentioned before, the core technologies behind AI empowering EDA are two milestone technologies, namely **reinforcement learning** and **large language models**.

First of all, reinforcement learning is mainly used for optimization problems in EDA, including optimal placement and routing, and test/verification vector generation. The main challenge of this type of problem is that the parameter optimization space is huge, and it is unrealistic to use brute force search to traverse all possible parameter combinations (for example, in layout problems, each logic gate in the design can be placed almost anywhere on the layout, for the current design with the number of logic gates easily reaching tens of millions, the violent search may not be completed until all life on the earth becomes extinct).

Traditional EDA uses heuristic algorithms such as annealing algorithms. It should be said that this type of algorithm has achieved great success. It has made the calculation time of placement and wiring problems controllable, thus creating the prosperity of today's chip field. The main advantage of the heuristic algorithm is that the calculation speed is faster and the calculation requirements are smaller, but it may not be able to find the globally optimal design parameters. On the other hand, the main principle of reinforcement learning is to learn the results of different parameter combinations from data, so that a more efficient parameter space search method can be learned in a data-driven manner. If the algorithm is properly designed and the training data is good enough, it can achieve better results than heuristic algorithms.

Deepmind 's AlphaGo defeated Lee Sedol in 2016 , it used a reinforcement learning model. This model learned from the massive amount of existing Go game data and was able to surpass humans. In fact, the optimization problem of Go is similar to the optimization problem of EDA. They are both in a huge search space (for example, in Go, each step has a very high degree of freedom, which leads to a large search space, while in EDA, the generation of test/verification vectors in layout and routing is similar) to find the optimal solution in an efficient manner. Therefore, in fact, during the time when AlphaGO was successful, there was already a lot of exploration in the academic community about using reinforcement learning in the field of EDA, and today we finally see reinforcement learning technology landing in the EDA field.

In addition to reinforcement learning, another key AI technology is the large language model. Its main help to the EDA industry is to help engineers speed up code writing and reduce the probability of errors. Large Language Model (LLM) represented by ChatGPT can understand users' needs expressed in natural language by learning rules from massive amounts of text, and generate natural language text that users can understand. The "natural language" here includes not only the language we usually speak, but also the programming languages we write, including Verilog, which is commonly used in circuit design. Currently, the most successful LLM-based code writing auxiliary tool is Github 's copilot , which can help users automatically complete the code (for example, after the user enters the first few characters of a line of code, copilot can predict what the user wants to write. What kind of code and prompt the user to automatically complete) and automatically find bugs in the code. We believe that by fine-tuning the large language model on the existing RTL code, it is very promising that a tool will emerge in the future to help chip design engineers quickly complete code writing, thus greatly improving the efficiency of engineers.

**How Will AI Affect the Work of Engineers?**

AI will further promote the development of the semiconductor industry. However, will chip engineers be robbed of their jobs by AI? We believe that, generally speaking, just as the emergence of EDA before did not take away the jobs of chip engineers, the next generation of AI-empowered EDA is mainly a tool to improve efficiency and will not replace human engineers.

First, let’s start from the field of front-end design. For chips, AI EDA mainly helps to use large language models to improve the code writing efficiency and quality of digital logic design. Therefore, there is no replacement relationship, but it provides a more convenient tool. For digital design engineers, the most essential job is to complete the circuit design, such as splitting a large system into multiple smaller functional modules, completing the function and interface definition of each module, and using code to implement these module. At present, the AI big language model mainly helps to complete the code, rather than directly writing the code; and even if AI can automatically write the code in the future, it cannot replace the essential work of the digital design engineer, which is to complete the definition of digital modules. and design.

In the field of back-end design, AI based on reinforcement learning can significantly improve the efficiency and quality of layout and routing. At present, the design process of most chips is that engineers first manually complete the high-level layout ( floorplan). After the estimated performance can reach the target, the EDA tool will then perform the next step of specific layout and routing, and the engineers will verify and fine tune it. We believe that as the efficiency and quality of layout and routing implemented by AI are further improved, floorplan work is likely to be increasingly handed over to EDA tools, and engineers' responsibilities will increasingly become to provide reasonable solutions to EDA tools. constraints and optimization goals, and verify the quality of designs generated by EDA tools. From this perspective, AI may indeed do more work that engineers currently do manually, but this does not mean that AI will replace these engineers, but that it can give these engineers additional responsibilities (i.e., provide tools with reasonable inputs and verified outputs), and improve overall efficiency. For other placement and routing processes, AI is more about providing a higher-quality tool and will not replace engineers.

In fact, AI may provide more jobs in the chip industry. We know that AI model training requires a large amount of data, and AI models may require different fine-tuning training for different designs. Therefore, the chip design industry may need more engineers who can optimize AI in a targeted manner.

**Industry Trends Brought About by EDA AI**

Finally, we analyze how AI will further empower EDA in the future.

First of all, the scale of chip design is getting larger and larger. From another perspective, the design search space is also getting larger and larger. In addition, as Moore's Law gets closer and closer to the physical limit, the overall industry 's requirements for chip design PPA are also getting higher and higher. Therefore, the use of AI to drive further improvements in chip design performance will be increasingly used, and we believe that where the design complexity and freedom are higher, AI can play a greater role. These areas include advanced packaging, especially 3D packaging; as well as mobile chips, high-performance computing chips and other fields that have very high requirements for chip design PPA - this is why we see companies such as Google and Nvidia that focus on high-performance computing chips. There is a lot of investment in the field of AI EDA . In the future, we expect that more such companies will use AI EDA to improve PPA.

In addition, another point worthy of attention is that AI may bring new changes to the industry, that is, AI requires a large amount of data to train. At present, the data of chip design is the intellectual property of each company. How to do it? Ensuring that the best model is trained while ensuring that intellectual property rights are not infringed is also an issue that needs to be addressed by the industry. We believe that large companies with a large amount of design accumulation will be the first customers to use AI EDA, because they can already train models with good performance based on their own design data. As for how small and medium-sized companies with less design accumulation or start-up companies with a short time of establishment use AI EDA will be a question worthy of consideration by the entire industry. For example, whether there will be some data sharing organizations to share some and It is possible to use less sensitive designs to train models together and use them together, or there are some methods based on encrypted computing training that can protect the design intellectual property as much as possible while allowing the model to use as much data as possible to complete the training. direction.

(Original text in Chinese machine translated with minor improvements)